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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/429,094	10/28/99	YATES J	30585/16

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EXAMINER	
ENG, D	
ART UNIT	**PAPER NUMBER**
2783	2

DATE MAILED: 07/18/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/429,094	Yates et al
Examiner	**Group Art Unit**
David Y. Eng	2783

☐ Responsive to communication(s) filed on _____

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire _____*three*_____ month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claim

☒ Claim(s) *1-23* is/are pending in the applicat

Of the above, claim(s) _____ is/are withdrawn from consideration

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-23* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____ .

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

— SEE OFFICE ACTION ON THE FOLLOWING PAGES —

Claims 1-23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

There is no functional relationship between the address translation circuitry and the other components. The pipeline, the table lookup circuit and the interrupt circuit or the handler have no use of the translated addresses.

It is not seen how the likelihood of the existence of an alternate coding of instruction (line 6, claim 1 for example) would cause the handler to affect the instruction pipeline circuitry to effect control of an architecture-visible data manipulation behavor or control transfer behavor of the instruction (line 15 of claim 1 for example). It appears that there is no relationship between them.

The claims fail to recite function of the address translation circuitry. It is not clear what type of address it is translated from and into.

In claim 4, the ISA 184 shown in Figure 1a is described in line 20 of page 39 as write-protect bit and not instruction set architecture as recited in claim 4. Applicant is requested to review the entire specification and drawings for any possible errors. Applicant is cautioned not to introduce any new matter.

With respect to all the claims, it is not seen why the interrupt to effect control of behavior of an instruction is triggered by memory state and instruction address.

Scope of limitation of the following claim languages is not clear:

cl 1 l. 15

1. "to effect control of an architecture-visible data manipulation behavor or control transfer behavior of the instruction". It is not clear what actually the instruction does.

2. "the architectural definition of the instruction not calling for an interrupt" in line 14 of claim 1.

The following have no clear antecedent basis:

1. "the address" in line 8 of claim 1. Is it the address of the memory location which stored the instruction or is it the source address or translated address from the address translater?

2. "execution control" in line 2 of claim 3. What is being executed or controlled and the execution cotrol of which is being transferred to a different instruction for execution? It appears that execution control of an instruction can not be transferred to a a different instruction for execution.

Other claims have similar all defects set forth above.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-13 and 19-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adachi (4,812,975).

Adachi discloses a microprocessor chip, comprising:

instruction pipeline circuitry (a plurality of first and second data processors, line 2 of the abstract),

a table and a table lookup circuitry (column 4, line 51) having entries for storing information,

an interrupt circuit and an interrupt handler for causing the pipeline to regard the instruction as an SVC instruction (lines 64 et seq of col 4) that can be processed on the target machine operating system and carries out the emulation to perform SVC operation as determined in accordance with the target machine architecture or to regard the instruction as an SVC instruction which is associated with an input/output control macro instruction in accordance with the information stored in the entry of the table.

It appears that in Adachi, the pipeline does not affect the instruction pipeline circuitry to effect control of an architecture-visible data manipulation behavor or control transfer behavor of the instruction. It is the position of the examiner that what actually an instruction is effect to control is a matter of design choice. What actually an instruction is effect to control is merely dependent on the individual instruction itself.

Claims 1 and 14-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adachi (4,812,975) in view of Bianchi (6,006,029).

Adachi discloses claim combination set forth above. Adachi does not appear to have an address translator. However, Bianchi discloses an emulator having an address translater (item 5 column 18). It would have been obvious to a person of ordinary skill in the art to incorporate an address translater in Adachi if addresses are required to be mapped or translated.

DAVID Y. ENG
PRIMARY EXAMINER